

a plurality of first selection/sense amplifier circuits including first selection means arranged in the respective regions between mutually adjacent pairs of said memory cell arrays for selecting one side at a time one of odd-numbered or even-numbered memory cell train out of the plurality of memory cell trains of the memory cell arrays on both sides of the regions between arrays, a plurality of amplifier means for amplifying in one-to-one correspondence the respective read data of memory cell trains selected by the first selection means, and second selection means for selecting one of the plurality of amplifier means and one of the memory cell trains selected by said first selection means and connecting them to corresponding data input and output lines, and transmit one of the amplified read data from a designated odd-numbered or even-numbered memory cell train of memory cell arrays on the selected one side to the corresponding data input and output lines and supply write data transmitted to the corresponding data input and output lines to selected memory cell trains of selected memory cell arrays; two units of second selection/sense amplifier circuits including a plurality of amplifier means arranged on the outside of the memory cell arrays on both ends of the arrangement of said plurality of memory cell arrays for amplifying in one-to-one correspondence the respective read data of odd-numbered or even-numbered memory cell trains of said memory cell arrays on both ends defined differently from the first selection/sense amplifier circuits corresponding to said memory cell arrays on both ends and connection means for selecting one of the plurality of the amplifier means and one of the designated odd-numbered or even-numbered memory cell array of said memory cell arrays on both ends and connecting them to corresponding data input and output lines, which transmit one of the amplified read data from the designated odd-numbered or even-numbered memory cell trains of the memory cell arrays on said both ends to said corresponding data input and output lines and supply write data transmitted to the corresponding data input and output lines from the external circuit to selected memory cell trains of said memory cell arrays on both ends; a plurality of data buses corresponding to each of the respective bits of data transferred in bit parallel mode between the external circuit; and a plurality of input and output switching circuits arranged in one-to-one correspondence to said plurality of first and second selection/sense amplifier circuits with their first input and output terminals connected to the data input and output lines of the corresponding selection/sense amplifier circuits and their second input and output terminals connected to one of said plurality of data buses so as to make the number of memory cell trains which makes the data transfer to the respective data buses, to carry out data transfer between each of said data buses and one of the corresponding selection/sense amplifier circuit;

wherein the number of memory cell trains capable of transferring data to the respective members of said plurality of data buses is set to be an even multiple of the number of said memory cell arrays, the second input and output terminals of the input and output switching circuits corresponding to said

9

second selection/sense amplifier circuits and the input and output switching circuit corresponding to the first selection/sense amplifier circuit arranged at the center of the first selection/sense amplifier circuits are connected to an identical data bus of the plurality of said data buses, and the second input and output terminals of the input and output switching circuits other than these input and output switching circuits are connected to the corresponding data buses so as to be laterally symmetric with respect to the connection line to the data bus of the input and output switching circuit corresponding to said first selection/sense amplifier circuit arranged at the center as the center line of symmetry.

2. A semiconductor memory device comprising:

a plurality of memory cell blocks each including a first and a second group of memory cells, said memory cell blocks being arranged in a first direction;

a first amplifier block provided adjacently to one end of an arrangement of said memory cell blocks, coupled to one of said first and second groups in one of said memory cell blocks on said one end, and selectively transferring a data of one of said memory cells in said one of said first and second groups via a first internal data line extending in a second direction different from said first direction;

a second amplifier block provided adjacently to another end of said arrangement, coupled to one of said first and second groups in one of said memory cell blocks on said another end, and selectively transferring a data of one of said memory cells in said one of first and second groups via a second internal data line thereof extending in said second direction;

at least one third amplifier block arranged between said memory cell blocks, coupled to one of said first and second groups in one of said memory cell blocks adjacent to one side thereof, and to one of said first and second groups in one of said memory cell blocks adjacent to another side thereof, and selectively transferring a data of one of said groups

545
170

10

coupled thereto via a third internal data line thereof extending along said second direction;
a first data line extending along said first direction and coupled commonly to said first and second internal data lines in said first and second amplifier blocks while being isolated from said third internal data line in said third amplifier block, said first and second amplifier blocks thereby being coupled to a common first input-output circuit via said first data line independently from said third amplifier block;
a second data line extending along said first direction and coupled to said third internal data lines in said third amplifier block and thereby coupling said third amplifier block to a second input-output circuit independently from said first and second amplifier blocks.

3. A semiconductor memory device comprising:

a plurality of memory cell blocks each including a first and a second memory cell;

a plurality of amplifier blocks, said memory cell blocks and said amplifier blocks being arranged alternately to form an array extending along a first direction, said array having on both ends thereof said amplifier blocks, thereby each of said memory cell blocks having both sides thereof on said first direction facing to said amplifier blocks, each of said memory cell blocks having said first and second memory cells thereof coupled to said amplifier blocks on one and another sides thereof, respectively;

a first data line for selectively connecting said amplifier blocks on said both ends of said array commonly to a first input-output circuit, thereby said first input-output circuit being associated with a first number of said first and second memory cells for read or write operation of said memory device;

a second data line for selectively connecting at least one of said amplifier blocks other than said amplifier blocks coupled to said first input-output circuit to a second input-output circuit, thereby said second input-output circuit being associated with said first number of said first and second memory cells for said operation of said memory device.

* * * * *

REISSUE APPLICATION OF U.S. PATENT NO. 5,444,305

1 4. A semiconductor memory device comprising:

2 a plurality of memory cell blocks each including a first and a second group of memory
3 cells, said memory cell blocks being arranged in a first direction;

4 a first amplifier block provided adjacently to one end of an arrangement of said memory
5 cell blocks, coupled to one of said first and second groups in one of said memory cell blocks on
6 said one end, and selectively transferring a data of one of said memory cells in said one of said
7 first and second groups via a first internal data line extending in a second direction different from
8 said first direction;

9 a second amplifier block provided adjacently to another end of said arrangement, coupled
10 to one of said first and second groups in one of said memory cell blocks on said another end, and
11 selectively transferring a data of one of said memory cells in said one of first and second groups
12 via a second internal data line thereof extending in said second direction;

13 at least one third amplifier block arranged between said memory cell blocks, coupled to
14 one of said first and second groups in one of said memory cell blocks adjacent to one side
15 thereof, and to one of said first and second groups in one of said memory cell blocks adjacent to
16 another side thereof, and selectively transferring a data of one of said groups coupled thereto via
17 a third internal data line thereof extending along said second direction;

18 a first data line extending along said first direction and coupled commonly to said first
19 and second internal data lines in said first and second amplifier blocks while being isolated from
20 said third internal data line in said third amplifier block; and

21 a second data line extending along said first direction and coupled to said third internal
22 data lines in said third amplifier block.

F 1 5. A semiconductor memory device as claimed in claim 4, further comprising a first
2 interface circuit coupled to said first data line and a second interface circuit coupled to said
3 second data line, said first and second amplifier blocks thereby being coupled to said first
4 interface circuit in common via said first data line independently from said third amplifier block.

REISSUE APPLICATION OF U.S. PATENT NO. 5,444,305

5 and said third amplifier block thereby being coupled to said second interface circuit
6 independently from said first and second amplifier blocks.

1 6. A semiconductor memory device as claimed in claim 5, wherein:
2 said first interface circuit operatively receives read data from one of said first and second
3 amplifier blocks; and
4 said second interface circuit operatively receives read data from said third amplifier
5 block.

1 7. A semiconductor memory device as claimed in claim 6, wherein said first and
2 second interface circuits operatively transfer write data to be written in said memory device.

1 8. A semiconductor memory device as claimed in claim 4, wherein:
2 each of said memory cell blocks has the memory cells thereof arranged in rows and
3 numbered columns to form a matrix, said columns including even and odd numbered columns;
4 each of said columns extends in said first direction;
5 for each of said memory cell blocks, said even numbered columns comprise one of said
6 first and second groups of memory cells, and said odd numbered columns include the other of
7 said first and second groups of memory cells.

1 9. A semiconductor memory device as claimed in claim 8, further comprising:
2 a plurality of sense amplifiers in each of said first, second and third amplifier blocks, each
3 of said sense amplifiers having a pair of input nodes; and
4 a plurality of pairs of parallel bit lines extending in said columns, one and another of bit
5 lines in one of said pairs of bit lines providing a reference potential and a read signal to be
6 applied to said sense amplifier, said sense amplifier in said third amplifier block having said pair
7 of input nodes thereof operatively connected to either one of said pairs of bit lines in one of said
8 memory cell block facing to one side of said third amplifier block and another pair of bit lines in
9 another memory cell block facing to another side of said third amplifier block.

REISSUE APPLICATION OF U.S. PATENT NO. 5,444,305

10. A semiconductor memory device as claimed in claim 9, further comprising:

a plurality of first pairs of transfer gate transistors each arranged between one of said pairs of bit lines and associated one of said sense amplifiers operatively providing a current path between one of said bit lines in said pair of bit lines and one of said nodes of said sense amplifier and simultaneously providing another current path between another of said bit lines in said pair of bit lines and another of said nodes of said sense amplifier in response to a transfer control signal.

11. A semiconductor memory device as claimed in claim 10, further comprising a

plurality of second pairs of transfer gate transistors each associated with one of said sense amplifiers in said first, said second and said third amplifier blocks, each of said pairs of second transfer gate transistors selectively providing a first current path between one of said nodes of said sense amplifier and one of said first, said second and said third internal data line and a second current path between another of said nodes of said sense amplifier and a complement data line associated with said one of said first, said second and said third internal data lines.

12. A semiconductor memory device comprising:

a plurality of memory cell blocks each including a first and a second memory cell;

a plurality of amplifier blocks, said memory cell blocks and said amplifier blocks being arranged alternately to form an array extending along a first direction, said array having on both ends thereof said amplifier blocks, thereby each of said memory cell blocks having both sides thereof on said first direction facing to said amplifier blocks, each of said memory cell blocks having said first and second memory cells thereof coupled to said amplifier blocks on one and another sides thereof, respectively;

a first data line coupled to said amplifier blocks on said both ends of said array commonly and associated with a number of said first and second memory cells for read or write operation of said memory device; and

a second data line coupled to at least one of said amplifier blocks other than said amplifier blocks coupled to said first data line, said second data line being isolated from said first data line and associated with said number of said first and second memory cells for said operation of said memory device.

REISSUE APPLICATION OF U.S. PATENT NO. 5,444,305

1 13. A semiconductor memory device as claimed in claim 12, further comprising a
2 first data transfer circuit coupled to said first data line and selectively coupled to said amplifier
3 blocks on said both ends of said array via said first data line, said first data transfer circuit being
4 associated with said number of memory cells, and a second data transfer circuit coupled to said
5 second data line and selectively coupled to said at least one amplifier block via said second data
6 line, said second data transfer circuit being associated with said number of memory cells.

1 14. A semiconductor memory device as claimed in claim 13, wherein said first and
2 second data transfer circuits receive read data of the memory device via said first and second data
3 lines.

1 15. A semiconductor memory device as claimed in claim 12, wherein each of said
2 memory cell blocks includes said memory cells arranged in rows and columns, said columns
3 extending in said first direction, one of said first and second memory cell belonging to an even
4 numbered column, another of said first and second memory cell belonging to an odd numbered
5 column.

1 16. A semiconductor memory device as claimed in claim 15, further comprising:
2 a sense amplifier in each of said amplifier blocks, said sense amplifier having a pair of
3 input nodes; and
4 a pair of bit lines in each of said columns, said pair of bit lines being arranged in a folded
5 bit line structure having one and another of said bit lines in said pair of bit lines providing a
6 reference potential and a read signal to be applied to said sense amplifier, said sense amplifier in
7 one of said amplifier blocks arranged between two of said memory cell blocks having said pair of
8 input nodes thereof operatively connected to one pair of bit lines in one column in either one of
9 said two memory cell blocks.

1 17. A semiconductor memory device as claimed in claim 16, further comprising:
2 a first pair of transfer gate transistors selectively providing current paths between said
3 pair of input nodes of said sense amplifier in one of said amplifier blocks arranged between two

REISSUE APPLICATION OF U.S. PATENT NO. 5,444,305

of said memory cell blocks and one pair of bit lines in one column in either one of said two memory cell blocks in response to a first transfer control signal; and a second pair of transfer gate transistors selectively providing current paths between said pair of input nodes of said sense amplifier and another pair of bit lines in another column in another of said two memory cell blocks in response to a second transfer control signal.

18. A semiconductor memory device as claimed in claim 17, further comprising:
a pair of signal lines extending in each of said amplifier blocks and in a second direction perpendicular to said first direction; and
a selection circuit in each of said amplifier blocks providing current paths between said input nodes of selected one of said amplifiers and said pair of signal lines according to a selection signal, said pair of signal lines being coupled to one of said data lines via a switching circuit.

19. A combination of amplifier blocks and memory cell blocks comprising:
N amplifier blocks arranged in a first direction, said N amplifier blocks including a first amplifier block, a last amplifier block, and a remainder of amplifier blocks;
N-1 memory cell blocks, each arranged between and coupled with two respectively adjacent ones of said N amplifier blocks, said remainder of amplifier blocks each being shared by two respectively adjacent ones of said memory cell blocks;
a first data line coupled to said first amplifier block and said last amplifier block; and
a second data line coupled to one of said remainder of amplifier blocks, said second data line being isolated from said first amplifier block and said last amplifier block.

20. A combination as claimed in claim 19, further comprising:
for each of said amplifier blocks, a respective signal line, extending in a second direction perpendicular to said first direction, for transferring a data signal from an associated one of said memory cell blocks;
said first data line being coupled, at a first side thereof, to said respective signal line of said first amplifier block;

REISSUE APPLICATION OF U.S. PATENT NO. 5,444,305

- 7 said first data line being coupled, at a second side thereof, to said respective signal line of
8 said amplifier block.

08046280-082297